ABSTRACT OF THE DISCLOSURE

The present invention discloses a method for manufacturing a nonvolatile memory transistor capable of minimizing the area when adapted to the technology of sub-micron. The method comprises the steps of: forming a trench of a predetermined shape on a silicon substrate; forming a N+ type doped region; etching the silicon substrate; forming ion implanted regions on the sides of the trench by conducting an inclined ion implantation for threshold voltage Vt control ion implantation of a select transistor; forming a poly-1 layer by depositing an oxide film and then depositing poly-1 serving as a gate node of the select transistor; after the formation of the poly-1 layer, conducting an etchback to the poly-1 layer; forming N+ ion implanted regions by conducting a N-type ion implantation in order to form a N+ source junction of a cell transistor; forming a channel of an EEPROM by additionally etching the silicon substrate; forming cell threshold voltage ion implanted regions by conducting an ion implantation in order to control the threshold voltage Vt of the channel of the cell; after the cell threshold voltage ion implantation, forming a cell gate oxide film by conducting the gate oxidation of the cell; forming a poly-2 layer by depositing poly-2 and then conducting an etchback; forming cell N-type drain junction regions by conducting an ion implantation in order to form a cell N-type drain junction; etching the poly-2 layer into a predetermined shape in order to form a control gate of the cell overlapped with the poly-2; forming a ply-3 layer by depositing an oxide film, depositing poly-3 and conducting an etchback; and filling an oxide film so as to be penetrated into the poly-3 layer, the oxide film, the poly-2 layer, the cell gate oxide film, the poly-1 layer and the oxide film under the poly-1 layer.